In the Claims:

1-7. (cancelled)

8. (currently amended) A bipolar transistor, comprising:

a collector including a frustum-shaped collector pedestal having an at least substantially planar upper surface, a lower surface, and a slanted sidewall extending between said upper surface and said lower surface, wherein said upper surface has an area substantially less than an area of said lower surface;

an intrinsic base overlying all of said area of said upper surface of said collector pedestal;

an emitter overlying said intrinsic base;

~~a raised~~ an extrinsic base conductively connected to said intrinsic base; and

a first dielectric region laterally adjacent to said emitter; and

a second dielectric region laterally adjacent to said collector pedestal, an opening extending through said first and second dielectric regions, said opening having a wall extending through said first and second dielectric regions, said emitter having an edge referenced to said wall of said opening and said collector pedestal having an edge referenced to said wall, such that said emitter is aligned with said collector pedestal.

~~extending along said slanted sidewall of said collector pedestal adjacent to said upper surface, wherein a centerline of said emitter is in alignment with a centerline of said collector pedestal~~.

9. (cancelled)

10. (previously presented) A bipolar transistor as claimed in claim 8, wherein said intrinsic base includes a layer of a single-crystal semiconductor which forms a heterojunction with at least one of said emitter and said collector pedestal.

11-20. (cancelled)

21. (currently amended) A bipolar transistor as claimed in claim ~~9~~ 8, further comprising a dielectric-filled shallow trench isolation and a conductive collector contact via, said collector further including a first active area and a second active area disposed in a single-crystal semiconductor region, each of said first and second active areas having major surfaces extending in lateral directions defining a major surface of said semiconductor region, said first active area underlying said collector pedestal and said second active area being separated in at least one of said lateral directions from said first active area by said shallow trench isolation, wherein said collector contact via overlies said second active area.

22. (new) A bipolar transistor as claimed in claim 8, wherein at least a portion of said extrinsic base is raised above an upper surface of said intrinsic base, wherein a wall of said raised portion of said extrinsic base is aligned with said wall of said opening in said first and second dielectric regions.

23. (new) A bipolar transistor as claimed in claim 22, further comprising a solid dielectric spacer spacing said raised portion of said extrinsic base from said emitter, said solid dielectric spacer including (a) a first dielectric spacer wholly contacting a wall of

said raised portion of said extrinsic base, and (b) a second dielectric spacer contacting an inner wall of said first dielectric spacer remote from said raised portion of said extrinsic base.